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CLAIMS

What is claimed is:

1. A method of measuring signal skew of a signal tree on a programmable logic device, the device including a signal tree having a source node connected to first, second, and third destination branches, first, second, and third logic blocks programmably connectable to the respective first, second, and third destination branches, each of the logic blocks having an input terminal and an output terminal, the method comprising:

   a. instantiating a first delay element on the device using a first programming sequence that includes:

      i. connecting the first destination branch to the input terminal of the first logic block; and

      ii. connecting the output terminal of the first logic block to the input terminal of the second logic block; and

   b. instantiating a second delay element on the device using a second programming sequence that includes:

      i. connecting the third destination branch to the input terminal of the third logic block; and

      ii. connecting the output terminal of the third logic block to the input terminal of the second logic block.

2. The method of claim 1, wherein the signal tree is a clock tree.

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3. The method of claim 1, wherein the input terminal of the second logic block is an asynchronous input terminal.

4. The method of claim 1, wherein the first, second, and third logic blocks are arranged on the device in a column.

5. The method of claim 4, wherein the second logic block is physically between the first and second logic blocks.

6. The method of claim 1, wherein the source node is further connected to fourth, fifth, and sixth destination branches and the programmable logic device further includes fourth, fifth, and sixth logic blocks programmably connectable to the respective fourth, fifth, and sixth destination branches, each of the logic blocks having an input terminal and an output terminal, the method further comprising:

c. instantiating a third delay element on the device using a third programming sequence that includes:

i. connecting the fourth destination branch to the input terminal of the fourth logic block; and

ii. connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block; and

d. instantiating a fourth delay element on the device using a fourth programming sequence that includes:

i. connecting the sixth destination branch to the input terminal of the sixth logic block; and

ii. connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block.

7. The method of claim 6, wherein connecting the output terminal of the first logic block to the input terminal of the second logic block establishes a first net, connecting the output terminal of the second logic block to the input terminal of the second logic block establishes a second net, connecting the output terminal of the fourth logic block to the input terminal of the fifth logic block establishes a third net, and connecting the output terminal of the sixth logic block to the input terminal of the fifth logic block establishes a fourth net, the method further comprising defining the first and third nets to be identical and defining the second and fourth nets to be identical.

8. The method of claim 1, further comprising configuring the device to include the first and second delay elements in respective first and second oscillators.

9. The method of claim 8, further comprising comparing the periods of the first and second oscillators.

10. A method comprising:

a. programming a programmable logic device to include a first delay element, the first delay element including:

i. a first destination branch connected to a clock source node;

ii. a first logic block having a first input terminal and a first output terminal, wherein the first input terminal is programmably connected to the first destination branch;

iii. a second logic block having a second input terminal and a second output terminal, wherein the second input terminal is programmably connected to the first output terminal; and

b. programming the programmable logic device to include a second delay element, the second delay element comprising:

i. a second destination branch connected to the clock source node; and

ii. a third logic block having a third input terminal and a third output terminal, wherein the third input terminal is programmably connected to the second destination branch and the third output terminal is programmably connected to the second input terminal.

11. The method of claim 10, wherein the first and second delay elements are portions of respective first and second oscillators.

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12. The method of claim 11, wherein the first oscillator includes a first net connected between the second output terminal and the clock source node, wherein the second oscillator includes a second net connected between the second output terminal and the clock source node, and wherein the first and second nets are identical.

13. The method of claim 10, wherein the first and second destination branches are parallel, and wherein the second logic block is disposed physically between the first and second destination branches.

14. The method of claim 13, further comprising a third destination branch parallel to the first and second destination branches, wherein the second logic block is programmably connectable to the third destination branch.

15. A method of calculating a first signal propagation delay along a portion of a signal distribution network on a programmable logic device, the method comprising:

d. instantiating a first delay element on the device using a first programming sequence, wherein the first delay element includes the portion of the signal distribution network;

e. determining a second signal propagation delay through the first delay element;

f. instantiating a second delay element on the device using a second programming sequence,

wherein the second delay element includes the portion of the signal distribution network; and

g. determining a third signal propagation delay through the second delay element.

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16. The method of claim 15, wherein the first signal propagation delay is proportional to the difference between the second and third signal propagation delays.

17. The method of claim 15, wherein instantiating the first delay element includes instantiating a first ring oscillator that includes the first delay element, and wherein instantiating the second delay element includes instantiating a second ring oscillator that includes the second delay element.

18. The method of claim 17, wherein determining the second and third signal propagation delays includes measuring the oscillation period of the respective first and second oscillators.